WHAT IS CLAIMED IS:

1. A method of performing built-in self repair of memories comprising:

making an on-chip assessment of amount of repair of a memory and flagging any memory as a fail when that memory exceeds a pre-determined limit.

2. The method as recited in claim 1, further comprising loading a counter with one or more values which establish a threshold for pass/fail criteria.

3. The method as recited in claim 2, further comprising loading the counter through a test pattern during production testing.

4. The method as recited in claim 1, further comprising loading a pre-determined repair solution into registers, testing the memories, and thereafter initiating the repair solution to repair the memories.

5. The method as recited in claim 4, further comprising using a reliability controller to test and control the number of repaired memories.

6. The method as recited in claim 5, said reliability controller comprising logic, at least one counter in communication with said logic, and a register set in communication with said logic.

7. The method as recited in claim 6, wherein said at least one counter comprises a first counter which contains the number of memories to be allowed for repair.

8. The method as recited in claim 7, further comprising loading a value into the register set which indicates the total number of memories.

9. The method as recited in claim 8, further comprising loading another value into the register set which indicates the maximum number of flare register bits among the memories.

10. The method as recited in claim 9, further comprising having the logic use the two values to create sections of patterns for each memory.

11. The method as recited in claim 10, wherein a start of each section contains redundant usage information.

12. A reliability controller configured for use in connection with built-in self repair of memories, said reliability controller configured to make an on-chip assessment of amount of repaired memories and flag any device failed when it exceeds a pre-determined limit.

13. The reliability controller as recited in claim 12, said reliability controller comprising logic, at least one counter in communication with said logic, and a register set in communication with said logic.

14. The reliability controller as recited in claim 13, wherein said at least one counter comprises a first counter which contains the number of memories to be allowed for repair.

15. The reliability controller as recited in claim 14, wherein the register set is configured to receive a value which indicates the total number of memories.

16. The reliability controller as recited in claim 15, wherein the register set is configured to receive a value which indicates the maximum number of flare register bits among the memories.

17. The reliability controller as recited in claim 16, wherein the logic is configured to use the two values to create sections of patterns for each memory.

18. The reliability controller as recited in claim 17, wherein a start of each section contains redundant usage information.